

WHAT IS CLAIMED IS:

- 1 1. A method of encoding a sequence of information bits in a communication
2 system comprising:
3 dividing said sequence of information bits into encoding bits and parallel bits;
4 encoding said encoding bits to produce encoded bits;
5 mapping said encoded bits and said parallel bits into first and second pulse
6 amplitude modulation (PAM) signals; and
7 generating a quaternary amplitude modulation (QAM) signal from said first and
8 said second PAM signals.
- 1 2. The method of claim 1, further comprising:
2 transmitting said QAM signal from said communication system associated with
3 said method of encoding.
- 1 3. The method of claim 2, wherein said communication system is an
2 asymmetric digital subscriber line (ADSL) communication system.
- 1 4. The method of claim 1, further comprising:
2 identifying whether a number of said information bits is odd or even.
- 1 5. The method of claim 4, further comprising:
2 selecting a mode of operation based on an odd or even status of said number of
3 said information bits.
- 1 6. The method of claim 5, wherein said mode of operation determines a
2 number of said encoding bits, a puncture pattern used in said encoding, a coding rate used in said
3 encoding, and a number of said encoded bits and said parallel bits used in said mapping.
- 1 7. The method of claim 5, wherein said selecting is made between a first
2 mode of operation and a second mode of operation.
- 1 8. The method of claim 4, wherein if a number of said information bits is
2 even, a number of said encoding bits is two.

- 1 9. The method of claim 4, wherein if a number of said information bits is
2 even, a number of said coding bits is greater than two.
- 1 10. The method of claim 4, wherein if a number of said information bits is
2 odd, a number of said encoding bits is three.
- 1 11. The method of claim 4, wherein if a number of said information bits is
2 odd, a number of said coding bits is greater than three.
- 1 12. The method of claim 1, wherein said encoded bits consist of systematic
2 bits and parity bits.
- 1 13. The method of claim 12, wherein if a number of said information bits is
2 even, a number of said systematic bits is two and a number of said parity bits is two.
- 1 14. The method of claim 12, wherein if a number of said information bits is
2 odd, a number of said systematic bits is three and a number of said parity bits is one.
- 1 15. The method of claim 1, wherein said encoding is performed by a turbo
2 encoder.
- 1 16. The method of claim 1, wherein said encoding is performed by multiple
2 turbo encoders.
- 1 17. The method of claim 1, wherein said encoding is performed by a serial
2 concatenated turbo encoder.
- 1 18. The method of claim 1, wherein said encoding is performed by a turbo
2 product code encoder.
- 1 19. The method of claim 1, wherein said encoding is performed by an low
2 density parity check (LDPC) encoder.
- 1 20. The method of claim 1, wherein said mapping includes:

2 forming a first vector and a second vector from said encoded bits and said parallel
3 bits.

1 21. The method of claim 20, wherein said mapping further includes:
2 mapping said first vector to said first PAM signal and mapping said second vector
3 to said second PAM signal.

1 22. The method of claim 20, wherein each of said first and said second vectors
2 is formed from alternate ones of said encoded bits and said parallel bits.

1 23. The method of claim 22, wherein said alternate ones of said encoded bits
2 form least significant bits and said alternate ones of said parallel bits form most significant bits
3 of each of said first and said second vectors.

1 24. The method of claim 1, wherein said mapping is a concatenated Gray
2 mapping.

1 25. The method of claim 24, wherein said concatenated Gray mapping is a
2 serial concatenation of an inner Gray mapping and an outer Gray mapping.

1 26. The method of claim 26, wherein said inner Gray mapping is applied to
2 said encoded bits and said outer Gray mapping is applied to said parallel bits.

1 27. An apparatus for encoding a sequence of bits in an asymmetric digital
2 subscriber line (ADSL) system, comprising:

3 a plurality of signal lines configured to divide said sequence of information bits
4 into encoding bits and parallel bits;

5 at least one turbo encoder configured to encode said encoding bits to produce
6 encoded bits; and

7 a quaternary amplitude modulation (QAM) unit configured to map said encoded
8 bits and said parallel bits into first and second pulse amplitude modulation (PAM) signals and to
9 generate a QAM signal from said first and said second PAM signals.

1 28. The apparatus of claim 27, further comprising:

2 a control unit configured to identify whether a number of said information bits is
3 odd or even.

1 29. The apparatus of claim 28, wherein said control unit is further configured
2 to generate a mode control signal based on an odd or even status of said number of information
3 bits.

1 30. The apparatus of claim 29, wherein said mode control signal is provided to
2 said at least one turbo encoder and said QAM unit to determine a number of said encoding bits, a
3 puncture pattern used in said encoding, a coding rate used in said encoding, and a number of said
4 encoded bits and said parallel bits used in said mapping.

1 31. The apparatus of claim 28, wherein if a number of said information bits is
2 even, a number of said encoding bits is two.

1 32. The apparatus of claim 28, wherein if a number of said information bits is
2 even, a number of said coding bits is greater than two.

1 33. The apparatus of claim 28, wherein if a number of said information bits is
2 odd, a number of said encoding bits is three.

1 34. The apparatus of claim 28, wherein if a number of said information bits is
2 odd, a number of said coding bits is greater than three.

1 35. The apparatus of claim 27, wherein said encoded bits consist of systematic
2 bits and parity bits.

1 36. The apparatus of claim 35, wherein if a number of said information bits is
2 even, a number of said systematic bits is two and a number of said parity bits is two.

1 37. The apparatus of claim 35, wherein if a number of said information bits is
2 odd, a number of said systematic bits is three and a number of said parity bits is one.

1 38. The apparatus of claim 27, wherein said at least one turbo encoder
2 comprises multiple turbo encoders.

- 1 39. The apparatus of claim 27, wherein said at least one turbo encoder
2 comprises at least one serial concatenated turbo encoder.
- 1 40. The apparatus of claim 27, wherein said at least one turbo encoder
2 comprises at least one turbo product code encoder.
- 1 41. The apparatus of claim 27, wherein said at least one turbo encoder
2 comprises a low density parity check (LDPC) encoder.
- 1 42. The apparatus of claim 27, wherein said QAM unit is further configured to
2 form a first vector and a second vector from said encoded bits and said parallel bits.
- 1 43. The apparatus of claim 42, wherein said QAM unit is further configured to
2 map said first vector to said first PAM signal and mapping said second vector to said second
3 PAM signal.
- 1 44. The apparatus of claim 42, wherein said QAM unit is further configured to
2 form each of said first and said second vectors from alternate ones of said encoded bits and said
3 parallel bits.
- 1 45. The apparatus of claim 44, wherein said QAM unit is further configured to
2 use said alternate ones of said encoded bits to form least significant bits and said alternate ones
3 of said parallel bits to form most significant bits of each of said first and said second vectors.
- 1 46. The apparatus of claim 27, wherein said QAM unit is further configured to
2 use a concatenated Gray mapping to map said encoded bits and said parallel bits.
- 1 47. The apparatus of claim 46, wherein said QAM unit is further configured to
2 implement said concatenated Gray mapping as a serial concatenation of an inner Gray mapping
3 and an outer Gray mapping.
- 1 48. The apparatus of claim 47, wherein said QAM unit is further configured to
2 apply said inner Gray mapping to said encoded bits and said outer Gray mapping to said parallel
3 bits.